

# CURRICULUM VITAE



**Name** Ali Jahanian  
**Position** Associate Professor  
**Affiliation** VLSI Design Automation Laboratory  
Computer Science and Engineering Department  
Shahid Beheshti University  
Velenjak, Tehran 19839-63113, Iran  
**Tel:** (+98) 21 29904188  
**Fax:** (+98) 21 22431804  
**E-mail:** jahanian@sbu.ac.ir , jahanian\_ali@yahoo.com

## Education

- **PhD. Student in Computer Engineering (Computer Systems Architecture)**  
From 2001, Amirkabir University of Technology, Tehran, Iran  
Graduated with GPA 22/20.0
- **M.S. in Computer Engineering (Computer Architecture)**  
1996 - 1998, Amirkabir University of Technology, Tehran, Iran. (GPA: 86 of 100)  
Graduated with GPA 17.17/20.0
- **B.Sc. in Computer Engineering (Hardware)**  
1992 - 1996, University of Tehran, Tehran, Iran. (GPA: 78 of 100)  
Graduated with GPA 15.66/20.0
- **Diploma in Mathematics & Physics**  
1988 - 1993, Ghods High School, Damghan, Iran. (GPA: 91 of 100)  
Graduated with GPA 18.12/20.0

## Honors and Awards

- Ranked 130 in Nation Wide Entrance Examination for Iranian Universities among about 300,000.
- Ranked 1 in B.Sc. in Tehran University.
- Ranked 1 in M.Sc. in Amirkabir University of Technology.
- The Top Researcher of *Iran Telecommunication Research Center* in 1997.
- Rank 5 in 10<sup>th</sup> International Memocode design contest, Arlington university, USA, 2012.
- Top Researcher of Shahid Beheshti University in 2013.
- Top Lecturer/Teacher of Shahid Beheshti University in 2013.
- Rank 1 in National Hardware Design contest-FPGA challenge, Sharif University, IRAN, 2013.
- Rank 1 in National Hardware Design contest-Layout design, Amirkabir University, IRAN, 2015.
- Rank 1 in Hardware Security challenge, Sharif University, IRAN, 2015.

## Research Interests

- Physical Design Algorithms
- Hardware security and trust
- CAD for Molecular computation systems

## Teaching

- Algorithms for VLSI design automation
- Hardware security and secure design
- System-on-chip design
- Principles of VLSI design
- Digital system design with VHDL

## Experiences

### **2013-Now**

- Management of Computer System Architecture Group in CSE department at Shahid Beheshti University.
- Contribution in foundation of Computer Science and Engineering department at Shahid Beheshti University.
- Experimental Implementation of the Microfluidic Biochips and DNA Computers.

### **2010-2013**

- Computer Group Management of ECE department at Shahid Shahid Beheshti University.
- Hardware security aspects of FPGA-based hardware design.
- Foundation of DNA Computing Laboratory at Computer Engineering Department of Shahid Beheshti University.

### **2010-2012**

- Computer Group Management of ECE department at Shahid Shahid Beheshti University.
- Design and implementation of SBU-FPGA prototype at Shahid Beheshti University.
- Foundation of Hardware Security R&D Laboratory at ECE department of Shahid Beheshti University.

### **2008-2010**

- Design and implementation of EduCAD Toolbox at Shahid Beheshti University.
- Foundation of VLSI Design Automation Laboratory at ECE department of Shahid Beheshti University.
- Teaching the under-graduate and graduate courses in Shahid Beheshti University.
- Participating to ECE department of Shahid Beheshti University.

### **2003-2007**

- Participated in Atlas physical design tool development as system designer and engine developer. Automatic Tool for Layout Synthesis (Atlas) is designed to do physical synthesis operation on design. It supports partitioning, floor-planning, placement and routing a digital standard cell design.
- Teaching the under-graduate courses in Amirkabir university of Tehran and Islamic Azad University (Ghazvin branch).
- Participated in design, implementation and test of Voice-over-IP chip design as system level designer and Media processor designer.

### **2000-2003**

- Participated in design, test, fabricate and post wafer testing the smart card chip for banking purposes. This chip is being used in Aber Bank ATMs.
- Participated in test, fabricate and post wafer testing the SIM card chip for GSM. This chip is going to going to be used in Iran GSM network (200,000 GSM Card).
- Design the smart card health-insurance application. The pilot scheme of this system was designed for *Taamin e Ejtemaei* (the main insurance company in Iran) to replace the booklet by smart card.
- Design, test and implement the memory card (phone card) compatible with *Infenion SLE5536* on FPGA board. This card is fully compatible with standard phone-card terminals.

### **1998-2000:**

- Design and implementation of switch-level VERILOG<sup>®</sup> base simulator to post-layout simulation.
- Design and implementation of full VERILOG<sup>®</sup> analyzer compatible with AIR<sup>®</sup> forma

- EDA Development Project manager in Emad Semicon Co.

#### **1996-1998:**

- Design and implementation and synthesis of a full LOAD/STORE RISC microprocessor for ATM switch routing.
- Design and implementation of *Hardware/Software C-VHDL Co-Simulator* tool for simulating the system level model of ATM switch
- Design and implementation of *Automatic Processor Interface Generator* for facilitating the automatic Hardware/Software Co-design process

### **Publications (after 2012)**

#### **Selected Journal Papers**

- Mehrshad Vosoughi and Ali Jahanian, Security-aware Register Placement to Hinder Malicious Hardware Updating and Improve Trojan Detectability, The ISC International Journal of Information Security, In press, (ISC- ).
- Hassan Daryanavard, Mohammad eshghi, and Ali Jahanian, A Fast Placement Algorithm for Embedded Just-In-Time Reconfigurable Extensible Processing Platform, Journal of Supercomputing, Vol. 171, pp: 121-143, 2015 (ISI-32383).
- Marzieh Morsehdzadeh and Ali Jahanian, Three-dimensional Switchbox Multiplexing in Emerging 3D-FPGAs to Reduce Chip Footprint and Improve TSV Usage, Accepted in Elsevier Integration the VLSI Journal, Vol. 50, pp: 81-90, 2015. (ISI-30485)
- M. Bakhsizadeh and A. Jahanian, Trojan Vulnerability Map: an Efficient Metric for Modeling and Improvement of Hardware Security Level , In IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E97-A, No.11, 2014.
- A.M. Zarei, A. Jahanian, RF Resource Planning in Application Specific Integrated Circuits to Improve Timing Closure, In CSI Journal on Computer Science and Engineering, 2014.
- Pishvaie, G. Jaberipur and A. Jahanian, High-performance CMOS (4:2) compressors, In Taylor & Francis International Journal of Electronics, DOI:10.1080/00207217.2014.880133, 2014.
- Z. Mohammadi-Arfa and A. Jahanian, Improved Delay and Process Variation Tolerance of Clock Tree Network in Ultra-large Circuits using Hybrid RF/Metal Clock Routing, In World Scientific Journal of Circuits, Systems, and Computers (JCSC), Vol.23, No.4, 2014.
- Belghadr and A. Jahanian, Metro-on-FPGA: a feasible solution to improve the congestion and routing resource management in future FPGAs, In Elsevier Integration the VLSI Journal, Vol. 47, No.1, 2014.
- Pishvaie, G. Jaberipur, and A. Jahanian, Redesigned CMOS (4; 2) compressor for fast binary multipliers, In Canadian Journal of Electrical and Computer Engineering, 2013, Vol.36, No.3, 2013.
- R. Abdollahi and A. Jahanian, Improved Timing Closure by Analytical Buffer and TSV Planning in Three-dimensional Chips, In Institute of Electrical, Information and Communication Engineers Transaction on Electronics, Vol. 9, No.24, 2012.
- Y. Zare and A. Jahanian, Improved Line Tracking System for Autonomous Navigation of High-Speed Vehicle, In International Journal of Robotics and Automation, Vol. 1, No.3, pp. 31-41, 2012.
- Pishvaei, G. Jaberipur, and A. Jahanian, Improved CMOS (4;2) compressor designs for parallel multipliers, In Elsevier Computers & Electrical Engineering, Vol. 12, No. 6, 2012.
- M. T. Teimoori, , A. Jahanian, and A. Dokhanchi, Performance Improvement and Congestion Reduction of Large FPGAs using On-chip Microwave Interconnects, In Institute of Electrical, Information and Communication Engineers Transaction on Electronics, , Vol. E95-c, No. 10, 2012.
- Farkish and A. Jahanian, Parallelizing the FPGA global routing algorithm on multi-core systems without quality degradation, In Institute of Electrical, Information and Communication Engineers Electronic Express Journal, Vol. 8, No. 24, 2012.

## Selected Conference Papers

- H. Daryanavard, A. Parvizian, A. Jahanian, and M. Eshghi, Design of CAD ASIP for JIT extensible processor: case study on Simulated Annealing placer, In 22th Iranian Conference on Electrical Engineering (ICEE), 2014.
- Taheri and A. Jahanian, Parallelizing the hyper-edge coarsening algorithm on GPU architecture, In 22th Iranian Conference on Electrical Engineering (ICEE), 2014.
- Haddad, M. Taajobian, and A. Jahanian, A new programmable architecture for microfluidic biochips, In 22th Iranian Conference on Electrical Engineering (ICEE), 2014.
- M. Jerengi, A. Jahanian, and M.H. Moayeri, A new cell library for Carbon nano-tube technology, In International CSI Computer Conference, 2014.
- A.M. Zarei and A. Jahanian, RF resource planning in application specific integrated circuits to improve timing closure, In CSI International Symposium on Computer Architecture and Digital Systems (CADS), 2013.
- Hosseiny, S. Amanollahi, R. Hashemi and A. Jahanian, Improved performance and resource usage of FPGA using resource-aware design: the case of decimal array multiplier, In CSI International Symposium on Computer Architecture and Digital Systems (CADS), 2013.
- S. Zamanzadeh and A. Jahanian, Improved hardware security in ASIC design flow using wire scrambling methodology, In International Conference on Very Large Scale Integration (VLSI-SoC), Turkey, 2013.
- Zarei and A. Jahanian, Performance improvement of ASICs using RF interconnect planning, In International CSI Computer Conference, 2013.
- M. Vosoooghi and A. Jahanian, Hardware Trojan avoidance using a new clock tree construction algorithm, In International CSI Computer Conference, 2013.
- Z. Mohammadi Arfa and A. Jahanian, Clock tree network using hybrid RF/metal clock routing , In Sharif Conference on Future Electronics, 2013.
- N. Ghasemian and A. Jahanian, A new nanowire-based FPGA to improve routing congestion and routability, In Sharif Conference on Future Electronics, 2013.
- Pourshirazi and A. Jahanian, RF-Interconnect resource assignment and placement algorithms in application specific ICs to improve performance and reduce routing congestion, In EuroMicro Digital System Design (DSD), 2012.
- S. Talebi and N. Abolghasemi, and A. Jahanian, EJOP: an extensible Java processor with reasonable performance/flexibility trade-off, In EuroMicro Digital System Design (DSD), 2012.
- S. Amanollahi and A. Jahanian, Edu3D: a simple and efficient platform for education of three-dimensional physical design automation algorithms, In Design, Automation and Test in Europe University booth (DATE), 2012.
- M. Morshedzadeh and A. Jahanian, Multiplexed switch box architecture in three-dimensional FPGAs to reduce silicon area and improve TSV usage, In Great Lakes Symposium on VLSI (GLSVLSI), 2012.
- M. Nasehi, A. Jahanian, and H. R. Zarandi, Modeling, evaluation and mitigation of SEU error in three-dimensional FPGAs, In CSI International Symposium on Computer Architecture and Digital Systems (CADS), 2012.
- F. Khoonbani and A. Jahanian, Improved performance and power consumption of three-dimensional FPGAs using Carbon Nanotube interconnects, In International Symposium on Computer Architecture and Digital Systems (CADS), 2012.
- M. Sanjabi, N. Miralaei, S. Amanollahi, and A. Jahanian, ParSA: parallel simulated annealing placement algorithm for multi-core systems, In International Symposium on Computer Architecture and Digital Systems (CADS), 2012.
- Marashi and A. Jahanian, TrueFlex: a flexible and efficient evaluation platform for networked automotive systems, In 20th Iranian Conference on Electrical Engineering (ICEE), 2012.
- N. Abolghasemi, S. Talebi, and A. Jahanian, Architecture and custom instructions for customizing the Java processor to improve execution performance, In 20th Iranian Conference on Electrical Engineering (ICEE), 2012.
- A. Pishvaei, G. Jaberipur, and A. Jahanian, 'Redesigned CMOS (4; 2) compressor for fast binary multipliers, In 20th Iranian Conference on Electrical Engineering (ICEE), 2012.
- Malekpour, S. Malekpour, and A. Jahanian, 'Design, implementation and improvement of decimal parallel multiplier on ASIC and FPGA, In 20th Iranian Conference on Electrical Engineering (ICEE), 2012.

## **Skills**

VHDL, Verilog, Modelsim, Synopsys Design Compiler, Cadence physical design tools, Magma tool, Leonardo, MaxPlus II, C++, ARM7 and 8051 Assembly

## **Hobbies**

Literature, Sports, Movies.